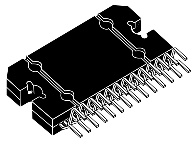
TDA7565

Quad power amplifier with integrated step-up converter

Features

- Multipower BCD technology
- DMOS power output
- Non-switching high efficiency amplifier
- Switching high efficiency voltage converter
- High output power capability:
  - 4 x 41 W max @ V_S = 14.4 V
  - 4 x 59 W @ V_S = 14.4 V and PWM = 17.5 V
- Full I^2C bus driving:
  - Standby
  - Independent front/rear soft play/mute
  - Selectable gain 26 dB - 12 dB (for low noise line output function)
  - High efficiency enable/disable
  - Voltage converter enable/disable
  - Regulated voltage selection
  - Switching frequency selection
- Hardware mute function
- Full fault protection
- DC offset detection
- Four independent short circuit protection
- Clipping detector with selectable threshold (1 % / 10 %) via I^2C bus



Flexiwatt27

Description

The TDA7565 is a new BCD technology quad bridge type of car radio amplifier in Flexiwatt27 package specially intended for car radio applications.

Thanks to the DMOS output stage the TDA7565 has a very low distortion allowing a clear powerful sound.

The built-in voltage converter control block assures a very high output power with an extremely low number of added components.

Furthermore, the converter makes the TDA7565 compliant to the most recent OEM specifications for low voltage operation (so called 'start-stop' battery profile during engine stop), helping car manufacturers to reduce the overall emissions and thus contributing to environment protection.

Table 1. Device summary

Order code	Package	Packing
TDA7565	Flexiwatt27	Tube

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1 Block and pin connection diagrams

Figure 1. Block diagram

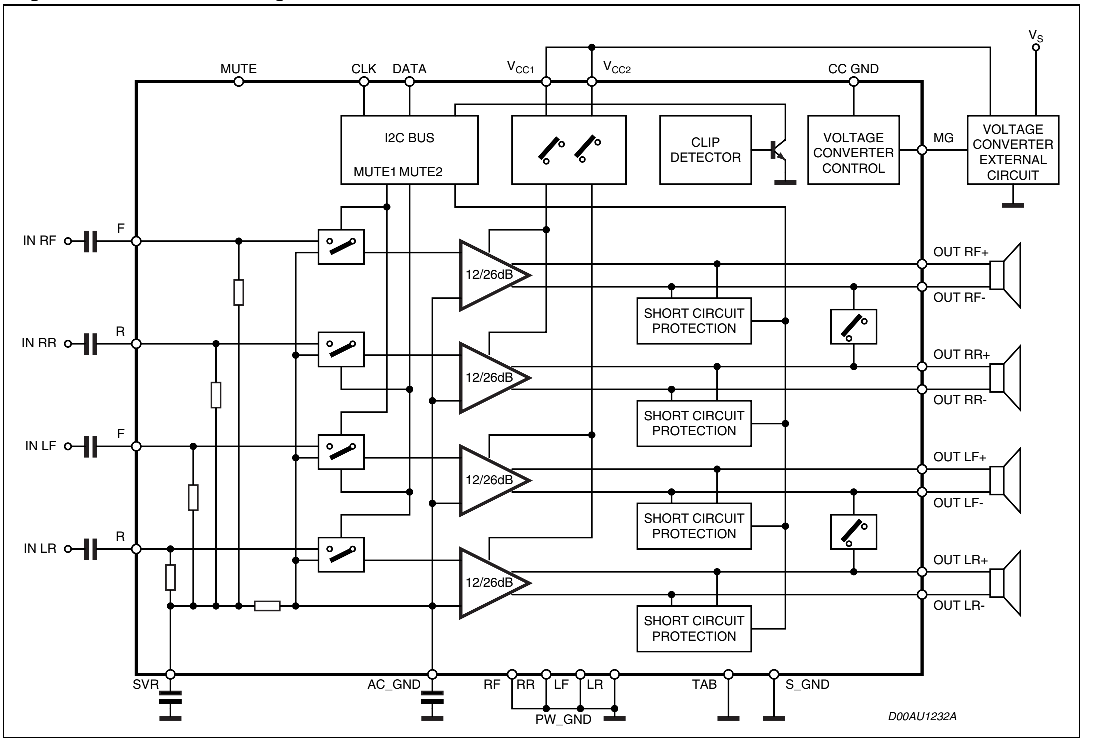
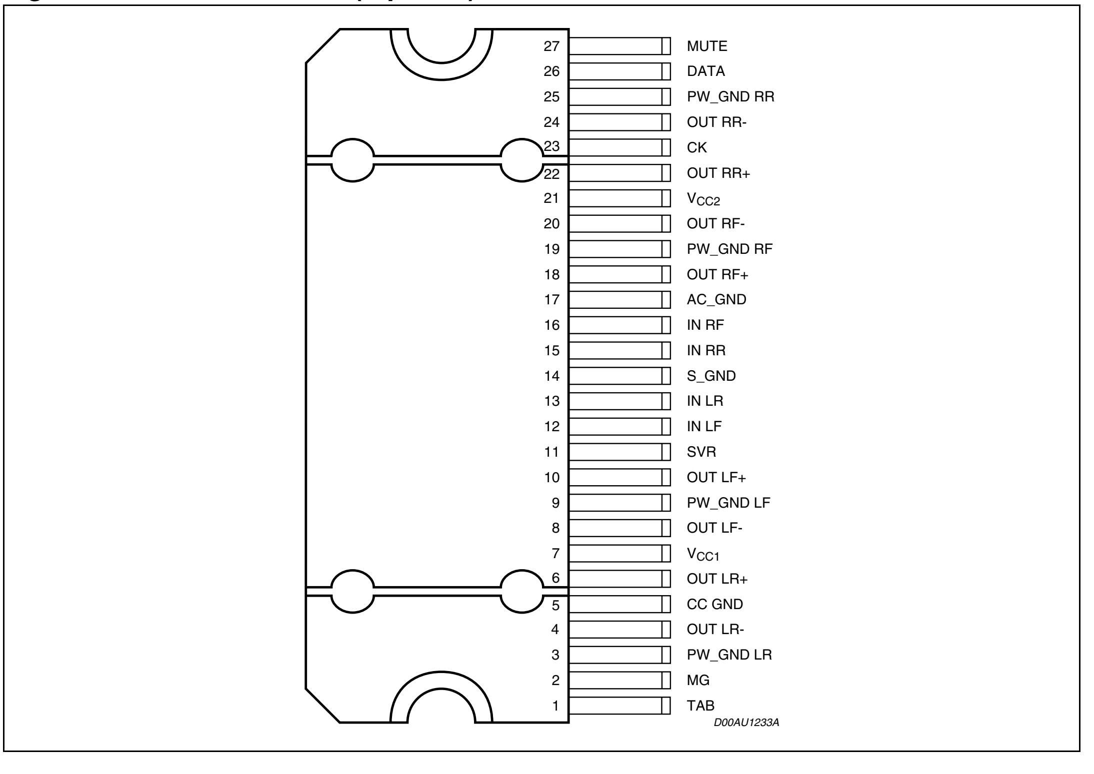


Figure 2. Pin connection (top view)



2 Electrical specification

2.1 Absolute maximum ratings

Table 2. Absolute maximum ratings

Symbol	Parameter	Value	Unit
$V_{opc\ OFF}$	Operating supply voltage, converter off	18	V
$V_{opc\ ON}$	Operating supply voltage, converter on	25	V
V_S	DC supply voltage	28	V
V_{peak}	Peak supply voltage (for t = 50 ms)	50	V
V_{CK}	CK pin voltage	6	V
V_{DATA}	Data pin voltage	6	V
I_O	Output peak current (not repetitive t = 100 µs)	8	A
I_O	Output peak current (repetitive f > 10 Hz)	6	A
P_{tot}	Power dissipation T_{case} = 70 °C	80	W
T_{stg}, T_j	Storage and junction temperature	-55 to 150	°C

2.2 Thermal data

Table 3. Thermal data

Symbol	Description		Value	Unit
$R_{th\ j\text{-}case}$	Thermal resistance junction to case	Max.	1	°C/W

2.3 Electrical characteristics

Refer to the test circuit, V_S = 14.4 V; R_L = 4 Ω; f = 1 kHz; voltage converter disabled (VC_{Off}); T_{amb} = 25 °C; unless otherwise specified.

Table 4. Electrical characteristics

Symbol	Parameter	Test condition	Min.	Typ.	Max.	Unit
Power amplifier						
V_S	Supply voltage range	-	8	-	18	V
I_d	Total quiescent drain current	-	-	250	300	mA
I_d	Total quiescent drain current (VC_{on})	-	-	350	-	mA
P_O	Output power (VC_{off}) V = 14.4 V	Max power[(1)]	-	41	-	W
		THD = 10 % THD = 1 %	22 18	27 22	-	W W

Table 4. Electrical characteristics (continued)

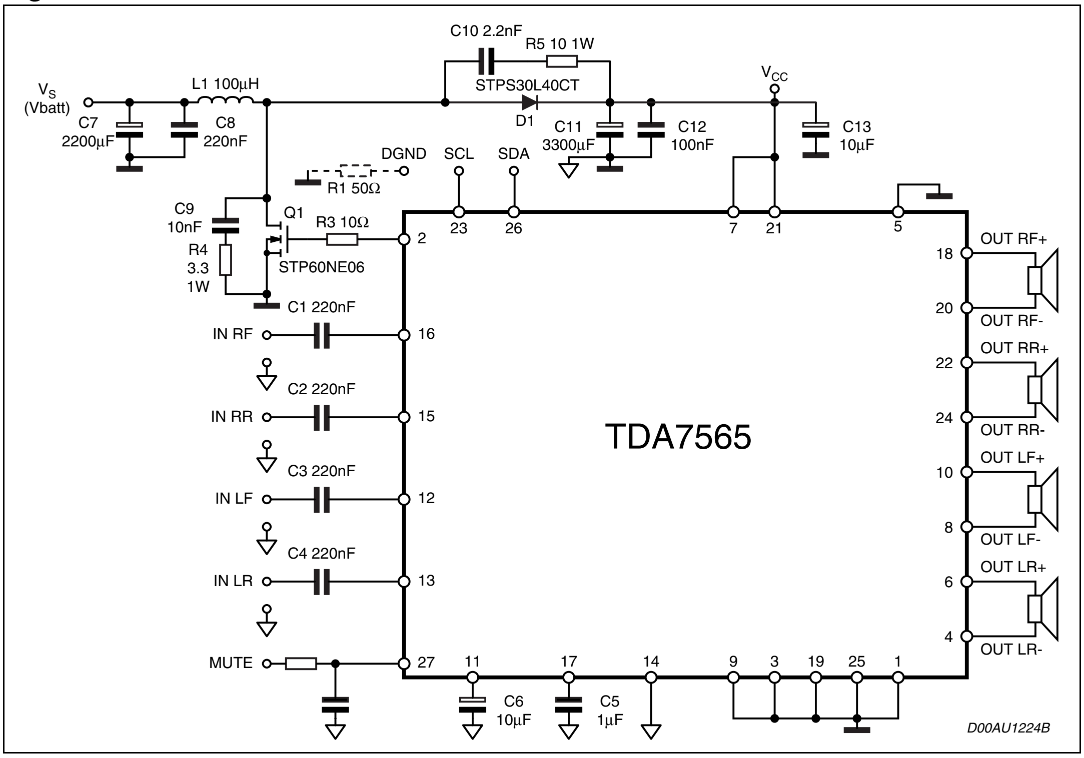
Symbol	Parameter	Test condition	Min.	Typ.	Max.	Unit
P_O	Output power (VC_{on}) V = 14.4V, PWM = 17.5V	Max power(1)	-	59	-	W
		THD = 10 % THD = 1 %	32 25	39 31	-	W W
THD	Total harmonic distortion	P_O = 1 W to 12 W; STDmode HE mode; P_O = 1-2 W HE mode; P_O = 4-12 W	-	0.03 0.03 0.1	0.1	% % %
		P_O = 1-12 W, f = 10 kHz	-	0.15	0.5	%
C_T	Cross talk	f = 1 kHz to 10 kHz, R_G = 600 Ω	50	55	-	dB
R_{IN}	Input impedance	-	60	100	130	KΩ
G_{V1}	Voltage gain 1	-	25.5	26	26.5	dB
ΔG_{V1}	Voltage gain match 1	-	-1	-	1	dB
G_{V2}	Voltage gain 2	-	11.5	12	12.5	dB
ΔG_{V2}	Voltage gain match 2	-	-1	-	1	dB
E_{IN1}	Output noise voltage 1	R_g = 600 Ω; G_V = 26 dB filter 20 Hz to 22 kHz	-	60	70	µV
E_{IN2}	Output noise voltage 2	R_g = 600 Ω; G_V = 26 dB filter 20 Hz to 12 kHz	-	15	25	µV
SVR	Supply voltage rejection	f = 100 Hz to 10 kHz; V_r = 1V pk; R_g = 600 Ω	50	60	-	dB
BW	Power bandwidth	(-3 dB)	75	-	-	KHz
A_{SB}	Standby attenuation	-	70	100		dB
I_{SB}	Standby current	-	-	-	50	µA
A_M	Mute attenuation	-	70	90		dB
V_{OS}	Offset voltage	Mute and play	-100	-	100	mV
V_{AM}	Min. supply voltage threshold	-	6.5	7	7.5	V
	Slew rate	-	1.5	-	-	V/µs
T_{ON}	Turn on delay	D2/D1 (IB1) 0 to 1	-	10	40	ms
T_{OFF}	Turn off delay	D2/D1 (IB1) 1 to 0	-	10	40	ms
-	Thermal foldback junction temperature	-	155	170	185	°C
CD_{THD}	Clip det thd. level	D0 (IB1) = 0	0	1	2	%
		D0 (IB1) = 1	5	10	15	%
V_O	Offset detection	Power amplifier = play AC Input = 0	±1.5	±2	±2.5	V
T_{hw}	Thermal warning	-	-	165	-	°C

Table 4. Electrical characteristics (continued)

Symbol	Parameter	Test condition	Min.	Typ.	Max.	Unit
I^2C bus interface						
f_{SCL}	Clock frequency	-	-	-	400	KHz
V_{IL}	Input low voltage	-	-	-	1.5	V
V_{IH}	Input high voltage	-	2.3	-	-	V
$V_{Min(pin27)}$	Mute in threshold voltage	Amp. mute	-	-	1.5	V
$V_{Mout(pin27)}$	Mute out threshold voltage	-	3.5	-	-	V
$A_{M(pin\ 27)}$	Mute attenuation	-	80	90	-	-
Voltage converter						
V_{cc1}, V_{cc2}	Converter output voltage (VC = ON)	V_S = 14 V D3 (IB2) = 0; D6 (IB2) = 0 D3 (IB2) = 1; D6 (IB2) = 0 D3 (IB2) = 0; D6 (IB2) = 1 D3 (IB2) = 1; D6 (IB2) = 1	-	 15 16.5 17.5 18.5	-	V
F_s	Voltage converter switching frequency	D6 (IB1) = 0; D7 (IB1) = 0 D6 (IB1) = 1; D7 (IB1) = 0 D6 (IB1) = 0; D7 (IB1) = 1 D6 (IB1) = 1; D7 (IB1) = 1	90 135 230 360	-	120 175 300 470	kHz
V_{mgl}	MOS gate output low voltage	I_o = 200 mA	-	1	2	V
V_{mgh}	MOS gate output high voltage	I_o = 20 mA	-	11	-	V
		I_o = 200 mA	-	9.5	-	V
$V_{mgclamp}$	MOS gate output clamp voltage	I_o = 5 mA	-	11.5	-	V
t_f	Fall time	C_o = 1 nF	-	20	-	ns
t_r	Rise time	C_o = 1 nF	-	50	-	ns
V_{mgl} (VC_{off})	MOS gate output voltage with voltage converter disabled	I_o = 5 mA	-	-	0.5	V

1. Saturated square wave output.

Figure 3. Demoboard schematic



3 I²C bus interface

Data transmission from microprocessor to the TDA7565 and vice versa takes place through the 2 wires I²C bus interface, consisting of the two lines SDA and SCL (pull-up resistors to positive supply voltage must be connected).

3.1 Data validity

As shown by *Figure 4*, the data on the SDA line must be stable during the high period of the clock. The HIGH and LOW state of the data line can only change when the clock signal on the SCL line is LOW.

3.2 Start and stop conditions

As shown by *Figure 5* a start condition is a high to low transition of the SDA line while SCL is HIGH. The stop condition is a low to high transition of the SDA line while SCL is high.

3.3 Byte format

Every byte transferred to the SDA line must contain 8 bits. Each byte must be followed by an acknowledge bit. The MSB is transferred first.

3.4 Acknowledge

The transmitter* puts a resistive high level on the SDA line during the acknowledge clock pulse (see *Figure 6*). The receiver** the acknowledges has to pull-down (low) the SDA line during the acknowledge clock pulse, so that the SDA line is stable low during this clock pulse.

* Transmitter

- master (µP) when it writes an address to the TDA7565
- slave (TDA7565) when the µP reads a data byte from TDA7565

** Receiver

- slave (TDA7565) when the µP writes an address to the TDA7565
- master (µP) when it reads a data byte from TDA7565

Figure 4. Data validity on the I²C bus

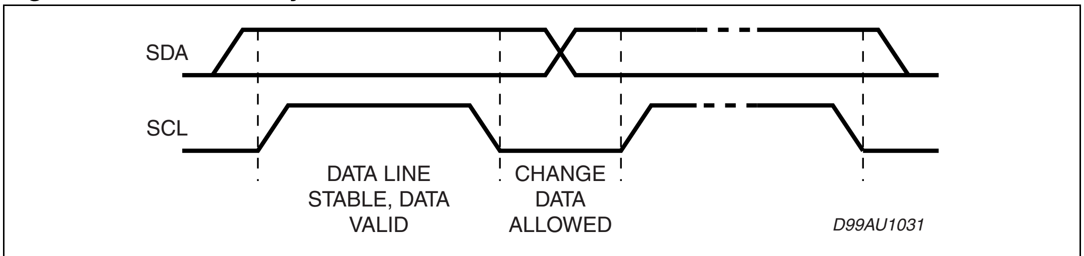


Figure 5. Timing diagram on the I²C bus

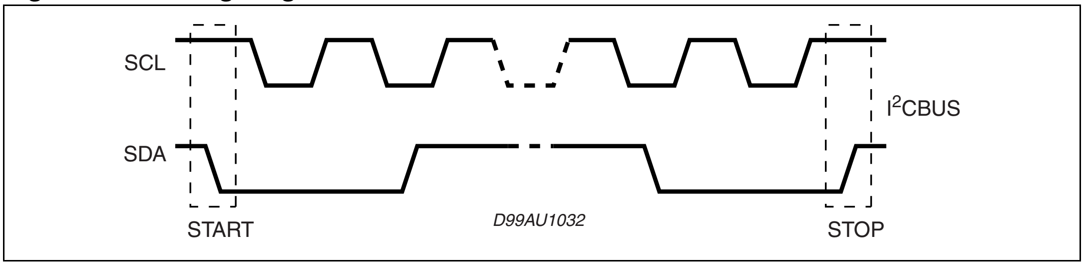
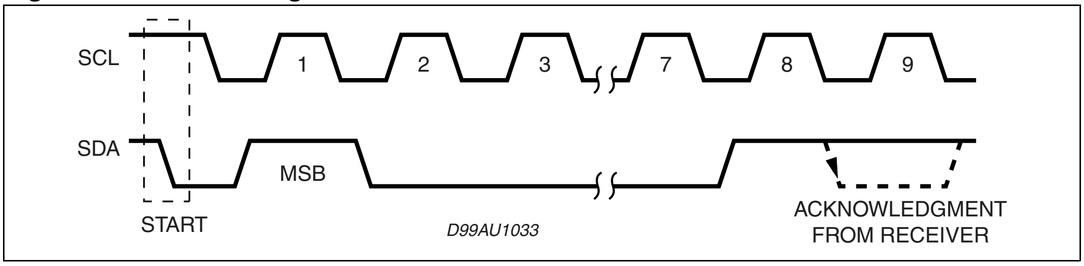


Figure 6. Acknowledge on the I²C bus



4 Software specifications

All the functions of the TDA7565 are activated by I^2C interface.

The bit 0 of the "ADDRESS BYTE" defines if the next bytes are write instruction (from µP to TDA7565) or read instruction (from TDA7565 to µP).

Table 5. Chip address

Bit	Instruction
D7	Address bit
D6	Address bit
D5	Address bit
D4	Address bit
D3	Address bit
D2	Address bit
D1	Address bit
D0(R/W)	Read/Write bit 0 = Write instruction 1 = read instruction

If R/W = 0, the µP sends 2 "Instruction Bytes": IB1 and IB2.

Table 6. IB1

Bit	Instruction
D7	Sel. freq. switch 1
D6	Sel. freq. switch 2
D5	Offset detection start (D5 = 1) Offset detection stop (D5 = 0) (off)
D4	Front channel Gain = 26dB (D4 = 0) Gain = 12dB (D4 = 1)
D3	Rear channel Gain = 26dB (D3 = 0) Gain = 12dB (D3 = 1)
D2	Mute front channels (D2 = 0) Unmute front channels (D2 = 1)
D1	Mute rear channels (D1 = 0) Unmute rear channels (D1 = 1)
D0	CD 1% (D0 = 0) CD 10% (D0 = 1)

Table 7. IB2

Bit	Instruction
D7	Voltage converter enabled (D7 = 1) Voltage converter disabled (D7 = 0)
D6	Regulated voltage selection 1
D5	Test speed
D4	Stand-by on - amplifier not working - (D4 = 0) Stand-by off - amplifier working - (D4 = 1)
D3	Regulated voltage selection 0)
D2	To be forced to “Level 1”
D1	Right channel Power amplifier working in standard mode (D1 = 0) Power amplifier working in Hi Eff. mode(D1 = 1)
D0	Left channel Power amplifier working in standard mode (D0 = 0) Power amplifier working in Hi Eff. mode(D0 = 1)

Table 8. DB1

Bit	Instruction
D7	Thermal warning
D6	X
D5	X
D4	X
D3	X
D2	Offset (LF)
D1	Short circuit protection (CH1)
D0	X

Table 9. DB2

Bit	Instruction
D7	Off status
D6	X
D5	Clip detector output
D4	X
D3	X
D2	Offset (LR)
D1	Short circuit protection (CH2)
D0	X

Table 10. DB3

Bit	Instruction
D7	Standby status
D6	X
D5	X
D4	X
D3	X
D2	Offset (RF)
D1	Short circuit protection (CH3)
D0	X

Table 11. DB4

Bit	Instruction
D7	X
D6	X
D5	X
D4	X
D3	X
D2	Offset (RR)
D1	Short circuit protection (CH4)
D0	X

5 Examples of bytes sequence

1 - Turn-on of the power amplifier with 26 dB gain, mute on, diagnostic defeat, high eff. mode, voltage converter disabled.

Start	Address byte with D0 = 0	ACK	IB1	ACK	IB2	ACK	STOP
			XX00X000		0XX1XX10		

2 - Turn-off of the power amplifier

Start	Address byte with D0 = 0	ACK	IB1	ACK	IB2	ACK	STOP
			XXXXXXXX		XXX0XXX0		

4 - Offset detection procedure start

Start	Address byte with D0 = 0	ACK	IB1	ACK	IB2	ACK	STOP
			XX1XX11X		XXX1XXX0		

5 - Offset detection procedure stop and reading operation.

Start	Address byte with D0 = 1	ACK	DB1	STOP

- The purpose of this test is to check if a D.C. offset (2V typ.) is present on the outputs, produced by input capacitor with anomalous leakage current or humidity between pins.
- The delay from 3 to 4 can be selected by software, starting from 1 ms

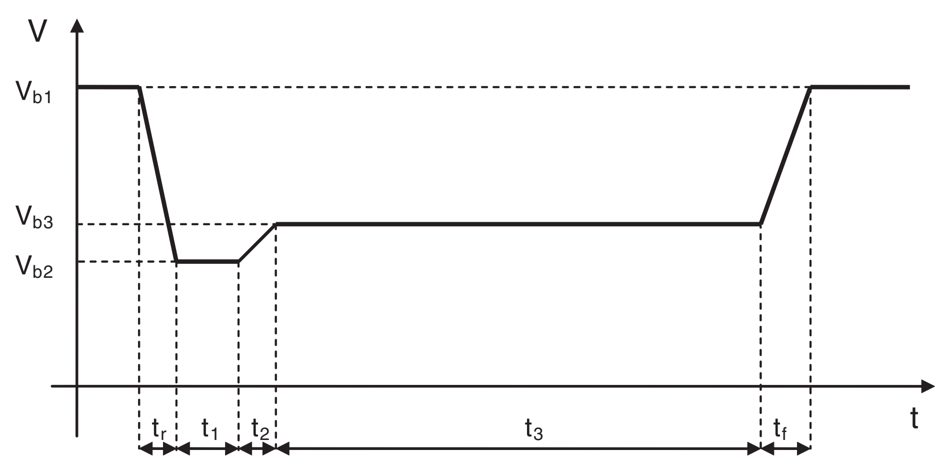
6 Low voltage "start-stop" operation

The most recent OEM specification are requiring automatic stop of car engine at traffic lights in order to reduce emissions of polluting substances. The TDA7565, thanks to its integrated switching voltage converter, allows a continuous operation when battery falls down to 6/7 V during such conditions, without producing pop noise. The maximum system power will be reduced accordingly.

The internal converter must be enabled and programmed in order to supply 15 V *(D3 (IB2) = 0; D6 (IB2) = 0)*. The suggested voltage frequency switching is 150 kHz *(D6 (IB1) = 1; D7 (IB1) = 0)*.

The following curve is a worst case condition for a start-stop system. The TDA7565, with the switching converter powered on, can sustain this cranking curve without any audio signal interruption.

Figure 7. Worst case condition for a start-stop system diagram



V_{b1} = 12 V, V_{b2} = 6 V, V_{b3} = 7 V

$R_i \leq 0.01\ \Omega$ (internal resistor of power supply)

Recovery time from test start to tr is 1 s

t_r = 2 ms

t_1 = 1 ms (the shortest time, at cranking simulation power supply, is 5 ms)

t_2 = 15 ms

t_3 = 1 s

t_f = 0.5 s

7 Package information

In order to meet environmental requirements, ST offers these devices in different grades of ECOPACK® packages, depending on their level of environmental compliance. ECOPACK® specifications, grade definitions and product status are available at: www.st.com.

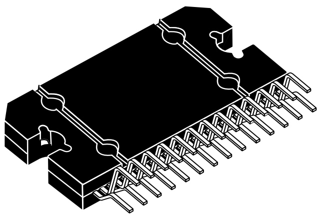
ECOPACK® is an ST trademark.

Figure 8. Flexiwatt27 (vertical) mechanical data and package dimensions

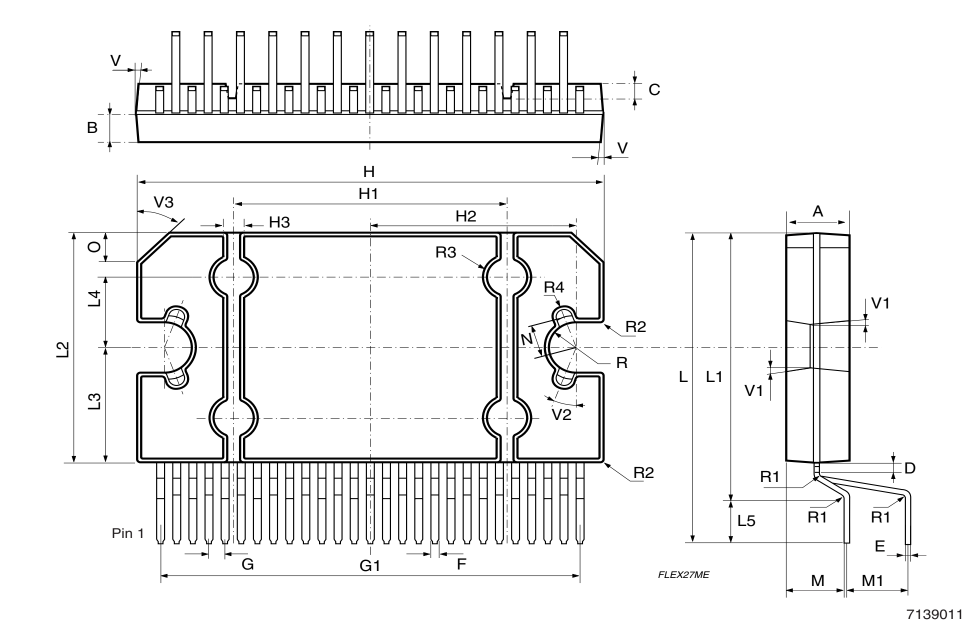
DIM.	mm			inch		
	MIN.	TYP.	MAX.	MIN.	TYP.	MAX.
A	4.45	4.50	4.65	0.175	0.177	0.183
B	1.80	1.90	2.00	0.070	0.074	0.079
C		1.40			0.055	
D	0.75	0.90	1.05	0.029	0.035	0.041
E	0.37	0.39	0.42	0.014	0.015	0.016
F (1)			0.57			0.022
G	0.80	1.00	1.20	0.031	0.040	0.047
G1	25.75	26.00	26.25	1.014	1.023	1.033
H (2)	28.90	29.23	29.30	1.139	1.150	1.153
H1		17.00			0.669	
H2		12.80			0.503	
H3		0.80			0.031	
L (2)	22.07	22.47	22.87	0.869	0.884	0.904
L1	18.57	18.97	19.37	0.731	0.747	0.762
L2 (2)	15.50	15.70	15.90	0.610	0.618	0.626
L3	7.70	7.85	7.95	0.303	0.309	0.313
L4		5			0.197	
L5		3.5			0.138	
M	3.70	4.00	4.30	0.145	0.157	0.169
M1	3.60	4.00	4.40	0.142	0.157	0.173
N		2.20			0.086	
O		2			0.079	
R		1.70			0.067	
R1		0.5			0.02	
R2		0.3			0.12	
R3		1.25			0.049	
R4		0.50			0.019	
V	5˚ (Typ.)					
V1	3˚ (Typ.)					
V2	20˚ (Typ.)					
V3	45˚ (Typ.)					

(1): dam-bar protusion not included
(2): molding protusion included

OUTLINE AND MECHANICAL DATA



Flexiwatt27 (vertical)



8 Revision history

Table 12. Document revision history

Date	Revision	Changes
20-Sep-2003	1	Initial release.
1-Jul-2008	2	Document reformatted. Document status promoted from product preview to datasheet.
25-Jan-2010	3	Updated *Features* and *Description on page 1*. Updated *Table 4: Electrical characteristics*. Added *Section 6: Low voltage "start-stop" operation*.
03-Feb-2010	4	Minor text changes.